A Confined Storage Nitride 3D NAND with Process Variation Effects on Cell Characteristics and Retention

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The explosive growth of AI workloads is driving an unprecedented need for higher bit density in NAND Flash. Aggressive vertical stacking (Z-scaling) has therefore become mandatory [1]. Confined charge storage-nitride (Confined SN) structures help enable such scaling by physically segmenting the SN, thereby mitigating cell-to-cell interference and improving retention reliability [2], [3]. Gate etchback, blocking oxide deposition, Si3N4 fill, and nitride pullback with liner reoxidation inevitably vary the storage nitride length (L_{sn}) [2]. Using TCAD simulations, we quantified how ±5 nm variations in L_{sn} influence program/erase (P/E) operation voltages and retention reliability characteristics. A ±5 nm shift in Lsn changes the P/E operation voltages by only about 0.5 V. In contrast, the same variation raises the Vertical Charge Loss (VCL—retention degradation caused by trapped charge leaking vertically from the SN into the channel) by roughly 10 %, showing that retention is far more sensitive to L_{sn} than P/E operation. Within this range, an optimal point emerges near $L_{sn} \approx L_{wl}$ (WL Gate Length)+4nm, where the required P/E operation voltage is reduced by approximately 0.3 V and the vertical charge loss(VCL) is lowered by about 10 % compared with the $L_{sn}=L_{wl}$ baseline. Consequently, variation in L_{sn} has little effect on P/E operation voltages, but it noticeably influences VCL, so optimizing L_{sn} is critical to reduce VCL degradation that inherently challenges Confined SN structures. This occurs because, when $L_{sn} > L_{wl}$, the trapped-charge density per unit L_{sn} falls, lowering the vertical electric field from SN to the channel and thereby reducing vertical charge loss. This study clarifies how process-driven variations in L_{sn} influence cell behavior. The resulting insights give engineers concrete design guidance: they can set realistic tolerances and fine-tune L_{sn} to curb vertical charge loss without compromising P / E performance. This approach optimizes confined SN structures for extreme Z-scaled, ultra-high-stack 3D NAND.

References

[1] Su Jin Ahn, Young Guen Song, Dongguk Cho, Daewon Ha, Wanki Kim, Kwangmin Park, Kwangjin Moon, Jin-woo Han, Seon Il Shim, Sangjin Hyun, and Jaihyuk Song, IMW (2025) pp. 1-4
[2] Chung-Hao Fu, Hang-Ting Lue, Tzu-Hsuan Hsu, Wei-Chen Chen, Guan-Ru Lee, Chia-Jung Chiu, Keh-Chung Wang, and Chih-Yuan Lu, IEEE Transactions on Electron Devices vol. 67, no. 3 (2020) pp. 989-994.
[3] Davide Resnati, Gianpietro Camevale1, Shyam Surthi, ChrisM. Carlson, Matthew Thorum, Terry Kim, Emilio Camerlenghi1 and Richard Hill, VLSI Technology and Circuits (2024) pp. 1-2.

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